REMARKS

Withdrawal of the finality of the last Office Action and formal acceptance of the amendment as a submission in connection with U.S. PTO RCE practice is respectfully requested. Reconsideration and allowance of the above-identified application, as currently amended, is also respectfully requested.

By the above-made amendments, independent claim 1, as well as dependent claims 4, 9-10, 17, 19, 23-24 and 26-28 were amended and claims 5-8, 11-16, 18, 21-22, 25 and 29-39 were cancelled, but, however, without prejudice or disclaimer of the subject matter therein. The amendments made to the claims are for purposes of effecting further clarification of the claimed subject matter, including with regard to the connection relationships of the constituent elements defined therein. In accordance with the above-made amendments, claims 1-4, 9-10, 17, 19-20, 23-24, and 26-28 are now pending. It is submitted, the invention as now set forth in independent claim 1 and, correspondingly, in the dependent claims thereof, as well as with regard to amended independent claim 28, could not have been rendered obvious in the manner alleged in the outstanding rejections. Therefore, insofar as presently applicable, the outstanding rejections, including the rejection of claims 1, 9, 11, 14-17, 21-23, 25 and 29-39 under 35 U.S.C. §103(a), allegedly, over the combination of Yamaguchi et al (USP 5,627,557) in view of Booth, Jr., et al (USP 6,648,915), the rejection of claims 2-8, 10, 18-20, 24 and 27 under 35 U.S.C. §103(a), allegedly, over the same combination of Yamaguchi et al and Booth, Jr., et al and further in view of Parks (USP 5,471,225), and also the rejection of claim 28 under 35 U.S.C. §103(a), allegedly, over the combination

of Yamaguchi et al in view of Zhang et al (USP 6,611,861), are traversed and withdrawal of the same is respectfully requested.

The present invention is for an image display apparatus which can display an image with a low power consumption. With regard to the present invention, low power consumption is achieved even when capacitance is used in the memory cells for storing an image data (i.e., a digital display data), noting that a field effect transistor (FET) is used as an amplifier in the individual memory cells. That is, since an amplifier using a FET is provided in each of the plurality of memory cells for storing digital display data, it thereby enables the read out of data accumulated in the respective capacitors of the memory cells to be performed under a low power consumption. This is in clear contradistinction with an apparatus such as illustrated in Fig. 19 of the drawings, which is discussed in the background section, in paragraphs [0005]-[0006] of the Specification. The construction in Fig. 19,which features a frame memory including DRAM cells and features, also, a sense amplifier (108) for reading out an image data from the memory cells, requires a large power consumption to display an image.

Specifically, the invention in amended claim 1 is an image display apparatus comprising:

> a plurality of signal lines;
>
> a plurality of display pixels arranged in a matrix to provide image display, each of said display pixels comprising a pixel electrode connected to said each of the plurality of signal lines via a pixel switch;
>
> a plurality of data lines;
>
> a plurality of memory cells for storing digital display data;

an image signal generating circuit for outputting an image signal to the signal lines based on said digital display data inputted from the plurality of memory cells via the data lines; and

wherein each of the plurality of memory cells comprises a memory switch; a memory capacitor connected to said memory switch; and a field-effect transistor of which a source-drain path thereof is provided between a first node and a second node coupled to a corresponding one of said data lines,

wherein one electrode of said memory capacitor is connected to a gate of said field-effect transistor and another electrode of said memory capacitor is connected to said second node, and

wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node.

Examples of the invention according to claim 1 are illustrated in connection with Figs. 1+, etc. of the present application, although not to be construed as being limited thereto. For example, reference 5 in Fig. 1 relates to the **plurality of signal lines** connected to the **display pixels** 10 which are arranged in a matrix, in which each display pixel 10 comprises a **pixel electrode** connected to a respective signal line like 5 via a **pixel switch** 2. In Fig.1 the **plurality of data lines** are shown in connection with reference 22 and the **plurality of memory cells for storing digital display data** are shown with regard to the memory cells 11, in which each is a memory cell for a three-bit image data. With regard to the individual memory cells according to claim1, FET amplifier 32 and FET switch 33 in example Fig. 1 relate to the set forth field-effect transistor and memory switch, respectively (see the discussion of Figs. 2 and 7 and memory cells 11 in connection with Fig. 1, etc.), although not to be construed as being limited thereto. Figs. 10 and 15 are other disclosed examples thereof, although not limited thereto. Various other example

showings of an image display apparatus in the drawings of the present application feature memory cells including an amplifier using a FET. Regarding the operation in Fig. 1, such as with regard to either a read or write cycle, a predetermined voltage is supplied to the first node such as a drain side of FET amplifier 32 in Figs. 2 or 10. In this memory cell construction, a predetermined voltage is provided through FET 61 in Fig. 1, as one example thereof. The operation, such as it relates to Fig. 1 of the drawings, as one example thereof, and in connection with a memory cell construction, such as shown in Figs. 2 or 10, is given beginning on page 13, paragraph [0045], of the Third Substitute Specification.

Another key aspect concerning the present invention such as defined in independent claim 1 and, therefore, also according to the dependent claims thereof calls for an "image signal generation circuit", an example of which is covered with regard to the digital-to-analog (DA) converter 6 and latch circuit 7 in the drawings. An example construction of the DA converter 6 as it relates to a three-bit memory cell 11 in Fig. 1 of the drawings is shown in Fig. 5 of the drawings, and regarding the latch circuit 7, examples thereof are given with regard to Fig. 3+, 13 and 17, although not to be construed as being limiting thereto. Various details regarding the constituent components set forth in independent claim 1 are featured with regard to the dependent claims thereof.

It is submitted, the invention according to independent claim 1 and, also, according to the corresponding dependent claims thereof could not have been achievable in accordance with that alleged in the outstanding rejections. For example, it is alleged that a memory element corresponds to that of a capacitor

in an image pixel. In this regard, it is observed that Yamaguchi et al, Booth, Jr., et al as well as Parks, call for a capacitor to an image pixel. This is clearly in contradistinction with that presently set forth. From the context of present independent claim 1, an image pixel which is represented by a display pixel (e.g., 10 in Fig. 1, etc.) is separate from that of a memory cell (e.g., 11), the constituent elements of which and specific connections thereof are now clearly set forth. Such it is submitted was neither taught by any of these applied references, and, moreover, could not have been suggested therefrom. Earlier pertinent discussions regarding Yamaguchi et al, Booth, Jr., et al, and Parks, in the responsive Remarks of the previous amendments, are also incorporated herein for purposes of this response.

Regarding the image display apparatus according to independent claim 28, the invention calls for, among the featured aspects thereof, a DA converter for outputting an image signal based on digital display data, in which the digital-to-analog converter is connected to a group of pixel electrode switches via a group of signal lines and the group of pixel switches are connected to the pixel electrodes of the corresponding display pixels. In accordance with the schemed construction in claim 28, the DA converter "contains a reference voltage generating circuit using a boron-doped polycrystalline Si (Poly-Si) thin-film resistor as a gray scale voltage generating resistor." It is submitted, the combined teachings of Yamaguchi et al and Zhang et al could not have suggested such a scheme.

Zhang et al, it is submitted, neither disclosed nor suggested a specific doping characteristic regarding the poly-Si thin film used therein. In fact, when

applying the combined teachings of Yamaguchi et al and Zhang et al, the resistance that would be realized would likely be prepared using phosphorus and arsenic doped poly-Si thin film. In contradistinction with this, as is set forth in claim 28, the poly-Si thin-film resistor is necessarily a boron doped poly-Si thin-film resistor [having low-dispersion sheet resistance] which leads to unexpected favorable results as that compared with, for example, a phosphorus doped poly-Si material (in regard to the formation of a thin film resistor). The more favorable attributes associated with a boron-doped poly-Si thin-film resistor are discussed in the present specification (see paragraph [0040] and Table 2 in the Specification). It is admitted in the rejection of claim 28 that "Yamaguchi et al fails [to teach] the specific usage of an image signal generating means, which has a reference voltage generating circuit using a poly-Si thin-film resistor as a gray scale voltage generating resistor." It is apparent therefore that both Yamaguchi et al and Zhang et al not only failed to teach a schemed construction as that called for in claim 28, but, moreover, the image display apparatus calling for especially a DA converter operatively connected as that presently set forth and which contains a reference voltage generating circuit using a boron-doped poly-Si thin-film resistor to achieve a gray scale voltage generating resistor could not have been realizable even in view of their combined teachings.

Therefore, in view of the above-made amendments, together with these accompanying remarks, favorable action on the pending claims and an early formal notification of allowance of the above-identified application is respectfully requested.

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To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. § 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (503.40029X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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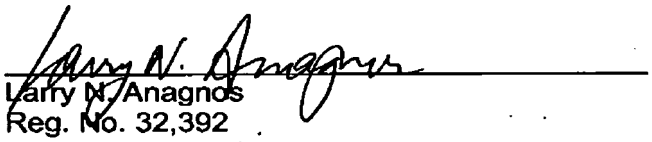

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Enclosures

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